501.40678CX1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):

J. NOGUCHI, et al

Application No.:

TBD

Filed:

December 23, 2003

For:

FABRICATION METHOD OF SEMICONDUCTOR

INTEGRATED CIRCUIT DEVICE

Expected Group:

2825

Expected Examiner: B. Keshavan

LETTER

Mail Stop Patent Application Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

December 23, 2003

Sir:

The sole claim of the above-identified application, claim 1, is noted. This claim 1 is the same as allowed claim 1 of Application No. 09/965,220, filed September 28, 2001, and is being submitted in order to provide a proper non-provisional application. Applicants will be filing a Supplemental Preliminary Amendment in due course, with claims to be considered on the merits in the above-identified application.

If the above-referred-to Supplemental Preliminary Amendment is not in the file of the above-identified application at the time that the Examiner takes up the above-identified application for consideration, the Examiner is respectfully requested to contact the undersigned so as to determine status of such Supplemental Preliminary Amendment. The Examiner is thanked in advance for complying with this request.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 501.40678CX1), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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WIS/sjg